CLAIMS

1. A data processing system, comprising:
   a first master;
   storage circuitry, coupled to the first master, for use by the first master;
   a first control storage circuit which stores a first prefetch limit;
   a prefetch buffer; and
   prefetch circuitry, coupled to the first control storage circuit, to the prefetch buffer, and to the storage circuitry, said prefetch circuitry selectively prefetches a predetermined number of lines from the storage circuitry into the prefetch buffer, wherein the first prefetch limit controls how many prefetches occur between misses in the prefetch buffer.

2. The data processing system of claim 1, further comprising:
   a first prefetch counter, wherein the prefetch circuitry selectively prefetches the predetermined number of lines from the storage circuitry into the prefetch buffer based on the first prefetch counter.

3. The data processing system of claim 1, further comprising:
   a second master, wherein the storage circuitry is coupled to the second master and is for use by the second master; and
   a second control storage circuit which corresponds to the second master and stores a second prefetch limit.

4. The data processing system of claim 3, wherein the first prefetch limit controls how many prefetches for the first master occur between misses in the prefetch buffer on read requests from the first master, and wherein the second prefetch limit controls how many prefetches for the second master occur between misses in the prefetch buffer on read requests from the second master.

5. The data processing system of claim 3, further comprising:

a first prefetch counter, wherein the prefetch circuitry selectively prefetches the predetermined number of lines for the first master from the storage circuitry into the prefetch buffer based on the first prefetch counter; and

a second prefetch counter, wherein the prefetch circuitry selectively prefetches a predetermined number of lines for the second master from the storage circuitry into the prefetch buffer based on the second prefetch counter.

6. The data processing system of claim 3, wherein the prefetch circuitry:

selectively prefetches the predetermined number of lines for the first master based on the first prefetch counter in response to at least one of a hit or a miss in the prefetch buffer corresponding to an access request from the first master; and

selectively prefetches the predetermined number of lines for the second master based on the second prefetch counter in response to at least one of a hit or a miss in the prefetch

buffer corresponding to an access request from the second master.

7. The data processing system of claim 1, wherein the prefetch circuitry selectively prefetches the predetermined number of lines in response to at least one of a hit or a miss in the prefetch buffer.

8. The data processing system of claim 1, wherein the first control storage circuit is programmable.

9. The data processing system of claim 1, further comprising a request monitor coupled to the first control storage circuitry, wherein the request monitor selectively updates the prefetch limit based on a number of buffer hits in the prefetch buffer accessed between two misses in the prefetch buffer.

10. A method for performing prefetch in a data processing system, comprising:

receiving a plurality of access requests from a master to access storage circuitry; and

using a prefetch limit to limit a number of prefetches performed between misses in a prefetch buffer resulting from at least a portion of the plurality of access requests.

11. The method of claim 10, further comprising providing a prefetch control circuit to store the prefetch limit.

12. The method of claim 10, wherein using the prefetch limit to limit the number of prefetches comprises:

counting prefetches after a miss in the prefetch buffer to determine when the prefetch limit is reached.

13. The method of claim 12, wherein each prefetch prefetches a single line from the storage circuitry.

14. The method of claim 13, wherein each single line prefetch is performed in response to at least one of a hit or a miss in the prefetch buffer.

15. A method for performing prefetch in a data processing system, comprising:

receiving a read request from a master to access storage circuitry;

determining whether the read request results in a hit or a miss in a prefetch buffer;

if the read request results in a hit, selectively performing a prefetch of a predetermined number of lines from the storage circuitry into the prefetch buffer based at least in part on a prefetch counter reaching a first value; and

if the read request results in a miss, performing a demand fetch in response to the read request and setting the prefetch counter to a second value.

16. The method of claim 15, wherein selectively performing the prefetch of the predetermined number of lines is further based on

whether or not the predetermined number of lines is already present in the prefetch buffer.

17. The method of claim 16, further comprising:

prefetching the predetermined number of lines from the storage circuitry and updating the prefetch counter when the read request results in a hit, the prefetch counter has not reached the first value, and the predetermined number of lines is not already present in the prefetch buffer.

18. The method of claim 17, wherein the second value corresponds to a prefetch limit and wherein updating the counter comprises decrementing the prefetch counter.

19. The method of claim 17, wherein the first value corresponds to a prefetch limit and wherein updating the counter comprises incrementing the prefetch counter.

20. The method of claim 16, further comprising:

not prefetching from the storage circuitry when the read request results in a hit and the prefetch counter has reached the first value.

21. The method of claim 15, further comprising prefetching a predetermined number of lines from the storage circuitry when the read request results in a miss.

22. The method of claim 15, wherein selectively performing a prefetch of a predetermined number of lines from the storage circuitry into the prefetch buffer based at least in part on a prefetch counter reaching a first value is performed such that the predetermined number of lines comprises only a single line.

23. The method of claim 15, further comprising:

receiving a master identifier corresponding to the master; and

selecting the prefetch counter from a plurality of prefetch counters based on the master identifier.